ABSTRACT OF THE DISCLOSURE

Generally, the present invention provides a system and method for processing instructions of a computer program and for indicating instruction attribute and/or status information so that the efficiency of the processing system may be increased. In architecture, the system of the present invention utilizes a pipeline, a scoreboard, and hazard detection circuitry. The pipeline processes and executes instructions of a computer program. Many of the instructions include register identifiers that identify registers where data should be written when the instructions are executed. When the data produced by execution of one of the instructions has yet to be written to the register identified by the one instruction's register identifier and is unavailable for use in executing other instructions of the program, the one instruction's register identifier is transmitted to the scoreboard. The scoreboard includes a plurality of multi-bit registers, and a first bit in one of the multi-bit registers is changed based on the received register identifier. The scoreboard also may receive data associated with the one instruction and may change a second bit in the one register based on the received data. Therefore, each register in the scoreboard indicates whether a pending write to a particular register exists and indicates information associated with the instruction causing the pending write.